Multi-Channel Transcutaneous Cortical Stimulation System

Contract # N01-NS-7-2365

Progress Report #7

for the contract period 10/31/98 – 1/31/99

Illinois Institute of Technology

Principal Investigator: Philip R. Troyk, Ph.D.

Introduction

The goal of this project is the design, fabrication, and testing of a ***Multi-Channel Transcutaneous Cortical Stimulation System*** to be used in a prototype artificial vision system**.** During the past 25 years, the development of a neuroprosthesis that could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This project uses the combined capability four organizations, the Illinois Institute of Technology, BioElectric Inc., Cross Technology, and the A.E. Mann Foundation to accomplish this challenging task.

This is the seventh progress report for this project. In this report we describe our progress on configuring deposition equipment for sealing of the ceramic package used in the 64-channel submodules and our progress on the ASIC designs.

Progress on Design of the Implant Package

In our sixth progress report we reported that we had evalued two types of glass for forming the glass-to-ceramic seals: a vitreous type (#41), and a crystalline type (#42). Both of the glasses have firing temperatures in the range of 370° - 380° C. This range is low enough to prevent deterioration of the thin-film metal which is to be used for interconnects and feedthroughs in the submodules. We prefer the #42 type glass because the crystalline type can be reheated without the glass returning to a liquid state. Since the sealing process involves 3 different seals, made in succession, we consider this an advantage.

During the last quarter we reported that we had made sample packages by depositing the glass, in the green state, using a commercially available oil-based vehicle. Our equipment was adapted from a modified X-Y plotter, and we were able to form seals of less than 0.04” wide, and less than 0.001” thick.

In this quarter, we continued testing the #42 glass for corrosion during high-temperature saline soak. Samples of the glass-to-glass sealed microscope slides have been soaking in 90° C saline since September of 1998. During this time we have seen no deterioration of the glass material, even under 500X microscopic examination. In addition, we have tested the sealed microscope slides for leaks, using a vacuum-bubble test. No leaks have been found, and no condensed water vapor is visible within the sealed area. These successes have raised our confidence about the integrity and reliability of the #42 glass seals. During the next few months we shall continue our investigation of the reliability of, and possible corrosion of, the low-temperature glass through more detailed analytical methods.

Although the modified X-Y plotter allowed us to produce test specimens and establish the feasibility of our glass seals, the glass deposition was variable and only moderate repeatability of seal patterns was possible. Therefore we obtained a numerical-controlled X-Y table as well as a screen printer. During this quarter we evaluated the suitability of this equipment to serve as a permanent glass deposition station.

The screen printer would allow precise control over the deposited glass width and pattern. However, we decided not to pursue this approach at this time. Screen printing requires larger volumes of the glass-vehicle mixture, than are needed for syringe deposition. Cleaning of the screen fixture is problematic, and undesirably large amounts of glass are wasted in the process. Rather, we have decided to use the X-Y table and air-powered syringe deposition. In the event that we are unable to obtain the desired control of the glass deposition, we will return to the screen printing method.

The X-Y table has a controller with an RS-232 interface. We have devised a software interface that permits direct use of AutoCad files to control the table. Presently we are machining fixtures to hold the syringe and position the ceramic and glass substrates so that we can obtain repeatable glass deposition. We expect the fixtures to be completed within the next month. At that time we shall resume fabrication of ceramic and glass prototype submodules and send to the Mann Foundation for helium leak testing.

We have also defined tooling patterns for alignment of the Macor substrates at Electrofilms and IIT. These tooling patterns are essential so that the metal deposition, on the ceramic, done at Electrofilms, can be aligned with the numerical-controlled milling operation of the substrates at IIT. During the next quarter we plan to test our patterns and alignment procedures on Macor substrates that will subsequently be glass-sealed using our X-Y table.

Progress on the design and fabrication of the submodule ASICs.

During the past quarter we have tested the ASIC BLOCK2 at NIH with actual IrOx metal electrodes. The first samples of the BLOCK2 chips that were fabricated as part of the A. E. Mann Foundation fall ’98 wafer was accomplished. We also analyzed BLOCK2 to better understand the consequence of photolithographic mismatching of equivalently-sized transistors. This resulted in the design, layout, and submission for fabrication of BLOCK3. Fabrication was accomplished by AMI through the MOSIS fabrication service.

Testing of BLOCK2 at NIH

During the first contract year, we had tested our design for the DAC electrode drivers at NIH, with metal IrOx electrodes. For clarity, we review that work below, and contrast those results with our latest testing

In order to test the performance of these early DAC circuits under actual electrode driving conditions, we designed a test platform for the MOS2 chips. The input address lines were interfaced to a hard-wired digital decoder circuit. The digital decoder circuit used hardware timers and address decoders to interface a Dallas DS5000 microprocessor to the MOS2 chips. A basic program (running on a PC), and communicating with the DS5000 over an RS-232 line, issued commands to the hardware controller and MOS2 chips. In this way we were able to produce an arbitrary combination of 4 channels of DAC outputs, each operating at their

individual pulse durations, frequencies, and current amplitudes. This test platform was tested at NIH during December of 1997. The output of the MOS2 chips were connected to microelectrodes and the electrode voltage-current relationships were examined.

The MOS2, chips used a method of charge recovery based upon the "shorting" of the DAC output for a brief time following the biphasic current pulse. The purpose of this technique was to compensate for cycle-to-cycle charge imbalances in the biphasic output drivers of the DAC. During our testing at NIH, we were able to access the consequences of this type of charge recovery. What we observed was that the inherent charge imbalance of the electrodes themselves was significantly larger than that caused by the DAC imbalance. At the end of each biphasic stimulation, a residual voltage remained on the electrode that was a function of the imbalance in the anodic and cathodic phases of the stimulus. It appeared that this voltage acted as an anodic bias so as to shift the electrode's operating point to one of less imbalance. The charge recovery switch created a large current, which served to discharge the electrode. Often this current would produce a cathodic bias on the electrode. Extensive measurements showed that this method of charge recovery would be potentially destructive to the electrodes.

During our testing, we observed that the residual charge imbalance, inherent to the electrodes, was a self-limited process, and there appeared to be no reason to attempt to recovery that charge. In fact, the residual charge tended to increase the anodic bias voltage in a direction that favored the electrode driving characteristics. What we did observe, however, was that when the DAC would be turned off for several minutes, the leakage current from the DAC output drivers was integrated by the output coupling capacitors, and those capacitors would charge until reaching the postitve, or negative, power supply. We decided that the electronic circuitry of the DAC needed to protect against long off-times of the DAC rather than for cycle-to-cycle charge recovery. Therefore what was needed was a linear regulator which used a low-level biphasic current regulator to maintain the DAC output at zero during the off-times.

We redesigned the DAC circuitry to eliminate the discharge switch and use a non-linear regulator whose output is limited to 0.5uA, and is used to maintain the DAC output near zero volts. During a normal current pulse the regulator is disabled. Following the biphasic pulse, the regulator is enabled. Simulations show that its performance should compensate for the "integration" effect of the output coupling capacitor and performance of the silicon chips, over the past six months, showed the regulator to function as expected.

BLOCK2 contains the complete address decoders, data latches, and timers that are needed for the final 8-channel Block chip designs. And with the exception of the electrode voltage-monitoring circuitry, all of the cells are near final-topology. BLOCK2 was interfaced to a microcontroller-based driver, designed to simulate the commands of the submodule state machine. The controller and 8-channel DAC chip, BLOCK2, was brought to NIH for testing in December of 1998. The results of those tests were highly encouraging. IrOx microelectrodes were driven from BLOCK2 for a variety of pulse amplitudes and durations. Anodic bias was applied externally using a NIH fixture. In each case, the electrodes showed no signs of changing waveshapes, and the BLOCK2 output regulator maintained the zero-bias state of the DAC outputs, even during long off periods.

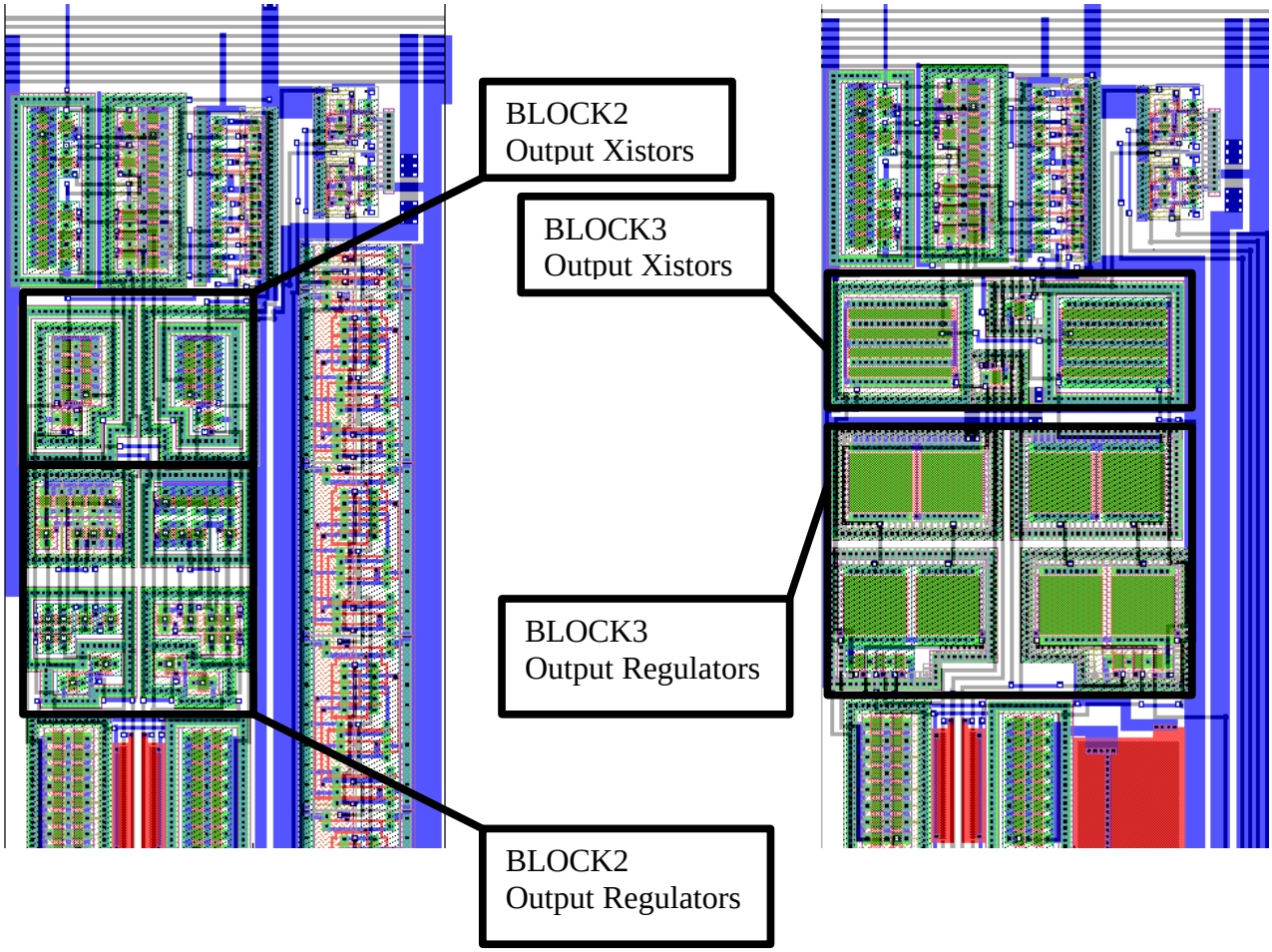
As a result of the Mann Foundation wafer run, a supply of over 100 of the BLOCK2 chips are available. These chips could be used in laboratory testing at NIH, and we intend to develop a compact micro-controller PC interface for driving them. We are evaluating the software previously used, at NIH, for controlling larger, rack-mounted, electrode drivers and

attempting to match our micro-controller to their software format. During the first half of 1999 we hope to deliver a number of DAC-controller combinations to NIH.

Design of BLOCK3

In spite of our success, during the NIH testing of BLOCK2, we continued to investigate the cause of the mismatch between identically designed DACs on the same die. In evaluating BLOCK2, we had found an improvement, over earlier designs, in the anodic-to-cathodic matching. For some DACs the match was as close as 2%. However, for other DACs the mismatch was larger, up to 15%. In order to achieve a wide compliance voltage range, we used a unique regulation of the current mirror voltages, as described in our last report. We had determined that variations in the offset voltage of the voltage regulators was responsible for the DAC-to-DAC variations.

We believe that these variations can be traced to lithographic differences between identical DAC stages on the same chip. We were impressed and surprised by our measurements that showed significant differences between identically-sized transistors, that we nearly adjacent to each other on the same die. Therefore, we included a Monte Carlo variation in the length and width of our transistor models in our SPICE computer simulations. Using this method, we concluded that a size increase of approximately six times was required for critical DAC transistors. We modified the DAC cells of BLOCK2 and submitted a new design, BLOCK3, for fabrication. In the figure below, the size change in the regulator and output transistors of BLOCK3, compared to BLOCK2 can be seen. Note the use of much larger transistors for the ones that need to be critically matched. We expect to receive this new ASIC during the next quarter.



Analysis of MOS10

Due to the year-end holidays, receipt of the MOS10 design from MOSIS was delayed. The chips are due by the middle of February 1999. We expect to analyze MOS10 during the next quarter. MOS10 contains circuitry for the electrode voltage monitors.